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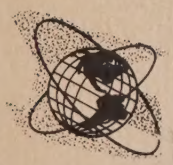
MODEL 4482 - FREQUENCY MEMORY

OPERATING INSTRUCTIONS & HANDBOOK

January 1969



Contract No. N62269-69-C-0007

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AIRBORNE INSTRUMENTS LABORATORY
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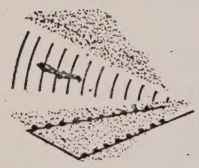

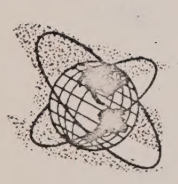

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Jim Dufort

916-595-3139

COUNTER MEASURES

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I. GENERAL INFORMATION

I - 1 Equipment Description

The Model 4482 Frequency Memory provides a CW output at the same frequency as a given pulsed input. When the input signal changes frequency from pulse to pulse, the Frequency Memory output also changes from pulse to pulse. In this case the Memory output is the frequency of the last input pulse. The complete specifications for the unit are given in Table 1.

I - 2 Equipment Application

The Frequency Memory is intended to be used for evaluation as an ECM system component for adaptation to an ECM system. The unit could work directly at the incoming frequency or as the intermediate frequency of a super-hetrodyne receiver. By proper selection of a local oscillator frequency, any RF frequency band could be covered by the IF frequency bandwidth. The CW output of the Frequency Memory would then be up-converted to the RF frequency. The same local oscillator would be used for the down-conversion.

II. PREPARATION FOR USE

II - 1 Power Considerations

The Model 4482 Frequency Memory may be operated from an AC source 105-132 volts at 45-440 cps.

II - 2 Power Connection

The Model 4482 Frequency Memory is provided with a three prong power cable which, when connected to an appropriate receptacle, grounds the equipment to the power line ground.

II - 3 Fuse

The 4482 Frequency Memory is supplied with a 2 amp fuse mounted in an indicating type fuse holder on the front panel. A spare fuse is also mounted inside the unit. See Figure 1.

III. OPERATING INSTRUCTIONS

III - 1 General

Plug in the AC line cord to an appropriate receptacle and switch on S1. This turns on the DC power supplies in the Model 4482 Frequency Memory. Allow 10 minutes for the memory to stabilize. Connect a signal generator, Hewlett-Packard 612 or equivalent, to the RF pulsed input port. See Figure 2. Set the modulation switch on the Hewlett-Packard 612 to the Pulse 2 position. The signal generator should be pulsed modulated from a Hewlett-Packard 214 pulse generator or equivalent. The signal generator should have a high on-to-off ratio to prevent CW leakage from going into the Memory. The pulse generator should be set to modulate the signal generator with a 1.0 microsecond pulse at 1,000 microseconds pulse repetition interval. The output of the signal generator should be -25 dbm minimum.

Connect the CW output port of the Model 4482 Frequency Memory to a spectrum analyzer, Hewlett-Packard 851B or equivalent. A 10 db attenuator or greater should be connected between the Frequency Memory output and the spectrum analyzer to prevent the local oscillator of the spectrum analyzer from feeding back into the Frequency Memory. See Figure 2. Set the spectrum analyzer frequency range to display a signal from 625-775 MHz. Two signals should be observed on the spectrum analyzer, one a CW signal, the other a pulsed signal ($\frac{\text{Sin X}}{\text{X}}$).

III - 2 Frequency Accuracy Check

Tune the frequency of the signal generator (Hewlett-Packard 612) across the band 625-775 MHz, observing the two signals on the spectrum analyzer; they should track over this frequency. Their error (distance between the peaks of the two signals) should not exceed 2 MHz.

III - 3 Number of Pulses for Initial Acquisition

Set the spectrum analyzer for a wide dispersion where a signal between 625 and 775 MHz can be observed. Set the pulse generator to a low PRF rate, approximately 2 PPS. Tune the signal generator to the low end of the band (625 MHz) and remove the pulse from the signal generator. Retune the signal generator to the high end of the band (775 MHz). Reconnect the pulse to the signal generator and count the number of pulses for initial acquisition from the low end of the band to the high end of the band by observing the

output on the spectrum analyzer. The number of pulses should be a maximum of 50. Repeat this procedure for the high end of the band. It also should be 50 pulses.

IV. PRINCIPLES OF OPERATION

IV - 1 General (See Figure 3)

The pulsed RF input comes into the Limiter (A1) where it is split equally by a two-way power divider. One of the outputs if fed to the Memory Threshold (A2) where it is detected, differentiated and amplified by a video amplifier. The video amplifier output triggers a monostable multi-vibrator which gates two switches "ON," the Memory Switch (S2) and the loop switch. The gain of the video amplifier is preset by a threshold control which fires the monostable multi-vibrator when the input signal level exceeds -25 dbm. Both switches (the loop switch and memory switch) remain "ON" for 800 nanoseconds regardless of input pulse width.

The other output of the power divider in the Limiter is used to update the Memory. This is the limited output. (Since the Frequency Memory design requires that the input signal has minimum amplitude variation, signal limiting is necessary.) The signal flows through the Limiter (A1), the Memory Switch (S2), the Bandpass Filter (FL1) and then to the Phase Discriminator (A4). The Limiter sets the signal at a specified level. The Memory Switch prevents transmission of undesired noise or spurious signals when a pulse is not present. The Filter rejects both harmonics of the Limiter output and the video transients generated by the Memory Switch.

Frequency memorization is accomplished by the loop circuitry, as shown in Figure 4. Its major components are a voltage controlled oscillator (VCO), a phase discriminator and a feed back loop. It operates in either one of two modes, the acquisition mode or the memory mode. The state of the loop switch determines the mode of operation. When it is closed the feed back loop will follow changes in the input frequency. This is called the acquisition mode. When it is open the loop is broken and the Frequency Memory is in the memory mode. The loop switch is located in the Memory Threshold (A2).

In the acquisition mode the loop switch closes for 800 nanoseconds whenever a signal is present. During this time, the VCO is tuned to the incoming frequency. Since the shortest anticipated pulse width is one microsecond and the time required to sense the pulse and switch the loop switch is about 200 nanoseconds, 800 nanoseconds is the maximum safe working time.

In the acquisition mode, the Frequency Memory is a frequency-locked loop, i.e. a small frequency error between the VCO natural frequency and the incoming pulse frequency is required to operate the loop. An error voltage is produced at the output of the phase discriminator which is proportional to the frequency difference between the input pulse and the natural VCO frequency.

The incoming pulse signal is split two ways in the input hybrid, one signal going to the Memory Oscillator to injection lock the oscillator to the incoming frequency; the other signal is fed to the phase discriminator. The injection locking of the oscillator is achieved by feeding into the output of the oscillator a signal level approximately 10 db below the oscillator's output power level. The oscillator frequency will be the impressed frequency as long as the signal power is fed into the oscillator. Thus, an oscillator with a natural frequency F0 can be made to oscillate at F1 by feeding a nominal amount of power at frequency F1 into the oscillator output.

During injection locking, there is a phase difference between the incoming signal F1 and the oscillator's output frequency F1. This phase shift is a function of the frequency difference of F1 and F0. It is this phase shift which produces the error voltage in the phase discriminator.

The output of the oscillator F1 is fed through a two-way power divider, one signal becomes the output of the unit, the other becomes one input to the phase discriminator. The two signals fed into the phase discriminator F1 (the signal frequency) and F1 (the oscillator's output frequency) are compared in phase. If $\emptyset$ is the phase difference between the impressed frequency F1 and the oscillator frequency F1, then the discriminator's output sin $\emptyset$ is proportional to the frequency difference of (F1 - F0). Thus, by measuring this phase difference, the frequency difference between F1 and the oscillator's natural frequency F0 is actually being measured. The voltage from the Phase Discriminator is fed to the Loop Amplifier which drives the varactor in the Memory Oscillator. The varactor voltages changes the natural resonant frequency of the oscillator from F0 to F1.

In the memory mode, the loop switch (and, therefore, the loop) is open. The Memory Oscillator can no longer change frequency because the injection input is removed (S2 OPEN) and the tuning input is removed. However, the oscillator will remain at F1 rather than returning to F0 because the memory capacitor has also been charged to the voltage corresponding to F1. Because of the low leakage paths in parallel with the memory capacitor, the capacitor will retain its charge until the next RF pulse is received. Therefore, the tuning voltage on the varactor, and thus the Memory Oscillator's frequency, will be constant between pulses. The system has thus "memorized" the frequency to the last input pulse.

IV - 2 Limited-Power Divider (A1)

The power divider is mounted in the Limiter chassis and is a toroidal core transformer. The Limiter is a seven stage transistor amplifier mounted on a printed circuit board in an aluminum chassis. Each stage is a broad band common emitter amplifier employing a 2N3571 transistor (see Figure 5). C1 is a coupling capacitor, C2 is used to bypass the emitter, CR1 is an HPA 2301 and is used for signal limiting. L1 and L2 match the input impedance of Q1. R1 is used to increase the amplifier stability. R2 and R3 are used to bias the stage at approximately 5 volts and 3 milliamps. All stages in the amplifier are similar to Figure 5 except the last stage which is biased at a higher level because of the power it must deliver (approximately 1 milliwatt). The output of the Limiter is flat to within $\pm$1 db with changes of amplitude and frequency.

IV - 3 Memory Threshold (A2)

The Memory Threshold contains a seven stage video amplifier preceded by a diode detector. The diode detector is flat within $\pm$1 db to insure a constant threshold level over the frequency band. The output of the video amplifier (which is adjustable and determines the threshold level) triggers a monostable multi-vibrator. The on-time of the multi-vibrator is 800 nanoseconds. The output of the multi-vibrator controls two drivers which drive the loop switch and the Memory Switch. The loop switch, which is in the Memory Threshold, is a 2N3970 field effect transistor. The Memory Threshold circuit is mounted on two printed circuit boards which are contained in an aluminum sheetmetal chassis.

IV - 4 Loop Circuitry

The loop circuitry is made up of two chassis, the Loop Amplifier (A3), Phase Discriminator and Memory Oscillator (A4). The Loop Amplifier is a nine stage wide band video amplifier with an adjustable voltage gain from 800-4000. Special care is taken with the design of this amplifier to prevent pulse stretching. Pulse stretching in the Loop Amplifier would result in the Frequency Memory overshooting the proper (input) frequency. The output of the Loop Amplifier must drive a relatively large capacitor (.056 UF - the memory capacitor). A 2N3026, which is a high power, high frequency transistor, is the last stage to drive the memory capacitor. The output of the Loop Amplifier is a pulse which varies from 0 to -8 volts. The Loop Amplifier components are mounted on a printed circuit board in an aluminum chassis.

The Phase Discriminator and Memory Oscillator assembly is composed of an isolation amplifier, a voltage controlled oscillator (VCO), a number of power dividers and a phase discriminator. The isolation amplifier is a single stage transistor amplifier with an adjustable gain similar to the stages in the Limiter. The isolation amplifier is used to isolate the phase discriminator from any variation in VSWR which would distort the response of the phase discriminator. A pin diode in the front end of the amplifier is used to control the gain of the stage. The isolation amplifier is built on a printed circuit board.

The unit contains three hybrids. One of these is used as a phase discriminator. All three hybrids are the toroid core type and are all mounted in a single sub-chassis. The phase discriminator uses two HPA 2349 Schottky barrier diodes in a bridge configuration.

The voltage controlled oscillator (VCO) is mounted on a printed circuit board. It utilizes a tunnel diode (AIL 33318-4) as an active element and a varactor (Parametrics Industries PV143B) element as a frequency tuning element. See Figure 6.

IV - 5 Bandpass Filter (FL1)

The bandpass filter is a 3 pole Chebishev inter-digital filter printed on a teflon fiberglass board. The insertion loss is less than 1.7 db and the VSWR is less than 1.6 across the band.

IV - 6 RF Switch

The RF Switch is a single pole, single throw pin diode switch. It uses an integrated circuit to drive the pin diodes. The driver requires a $+3.5 \pm .5$ volt control signal to turn it on and 0 to $\pm .5$ volt signal to turn off. The on-to-off ratio is 40 db minimum and the insertion loss of the switch is 1 db maximum. The switching time is 80 nanoseconds maximum.

IV - 7 Power Supplies

The 4482 Frequency Memory uses three Lambda power supplies, a $+4$ volt supply, a $+22$ volt supply, and a -22 volt supply. Each power supply is adjusted to ± 1 percent of the nominal voltage. The three supplies require an input of 115 VAC. The DC output of the supply has a .03 percent regulation from no load to full load. The power supplies are housed in a steel chassis which is perforated for ventilation.

V. MAINTENANCE

All of the controls in the Model 4482 Frequency Memory have been pre-adjusted and no adjustment should be necessary. However, if the unit fails to function the following procedure should be followed:

Trouble Shooting:

1. No CW output:

(a) Check power supply for proper DC outputs. Also check DC voltages to Phase Discriminator (A4).

(b) Check RF cable from Phase Discriminator output to front panel. If still no CW then the Memory Oscillator is inoperative if (a) and (b) correct. The replacement and alignment of this oscillator is critical to the performance of the loop, therefore, personnel familiar with this alignment should replace the Memory Oscillator.

2. CW output but unit does not track:

(a) Check the Memory Switch drive signal (a positive pulse of 800 nanoseconds at $\neq 3$ to $\neq 4$ volts) either at the Memory Threshold or at the control on the Memory Switch. If the drive signal is present go to step (c). If the drive signal is not present the Memory Threshold is inoperative or there is no input to the Memory Threshold.

(b) Check the input to the Memory Threshold on the spectrum analyzer. It should be a pulsed signal at -28 dbm. If there is a signal present on the analyzer, the Memory Threshold is inoperative. In replacing the Memory Threshold the gain adjustment on the Memory Threshold has to be readjusted. With a -28 dbm pulsed signal (1.0 microseconds) into the J1 port of the Memory Threshold. Adjust the gain pot until the Memory Threshold just fires the Memory Switch.

(c) Memory Switch drive signal present at switch control port. Check the input and output of the Memory Switch using a crystal detector. A -1 dbm pulse approximately 800 nanoseconds wide should be observed.

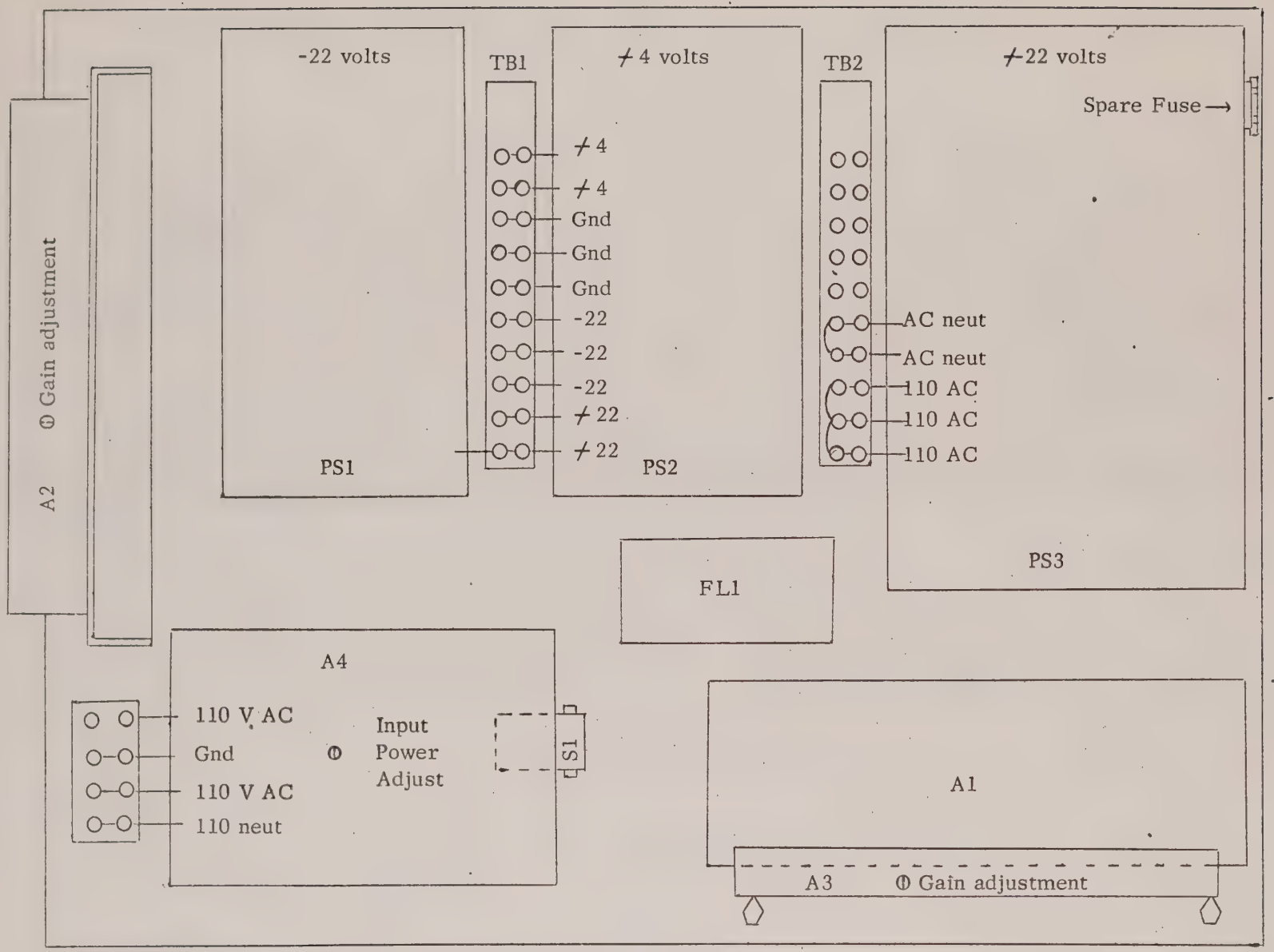
(d) No input to Memory Switch. If no output from the Limiter, the Limiter is inoperative (replace).

(e) Output from Memory Switch. If the output of the Memory Switch is correct (step c), check input and output of bandpass filter. If no output is obtained, filter is inoperative (replace).

(f) Output from bandpass filter. If the output of the filter is correct, then the Phase Discriminator is inoperative or loop amplifier is inoperative. To check the Loop Amplifier see Figure 7. If there is no input to the Loop Amplifier, the Phase Discriminator is inoperative. This unit, because of critical adjustments, must be replaced by personnel familiar with the unit.

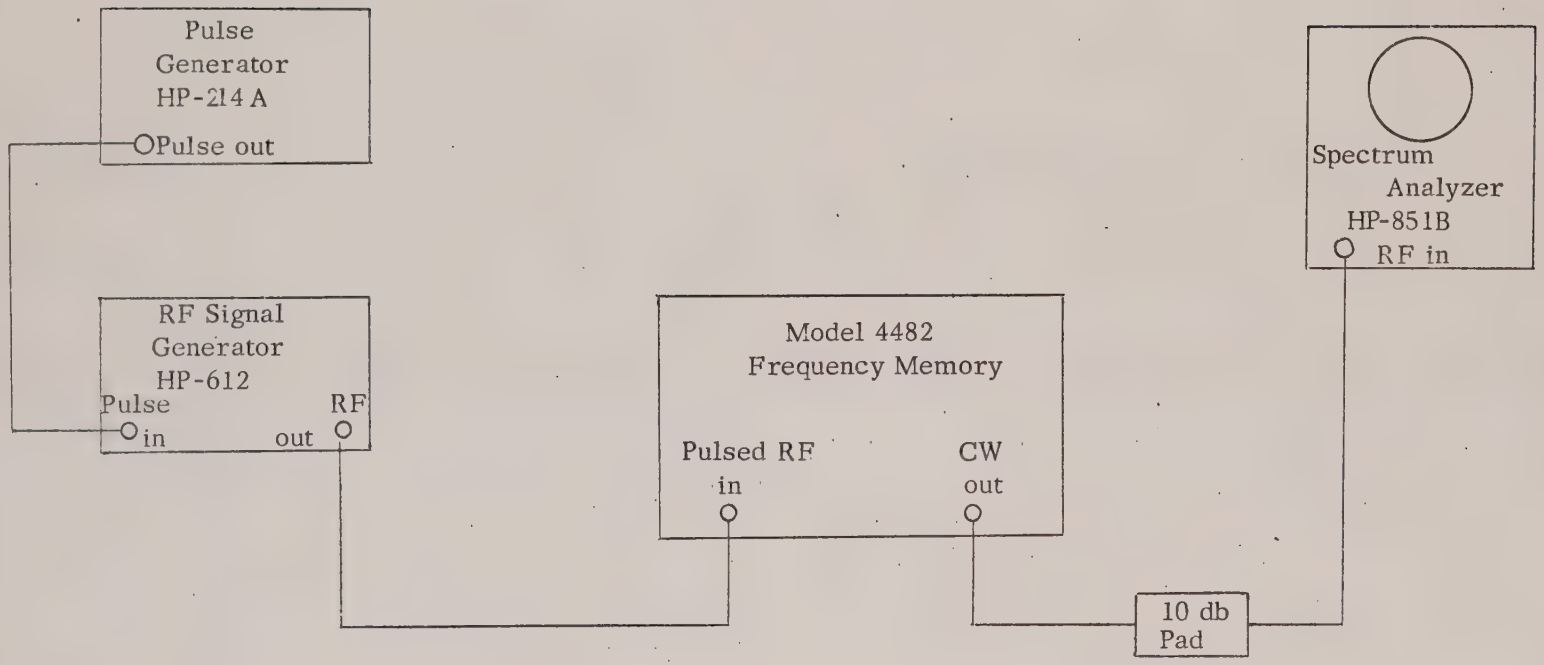
In replacing the Loop Amplifier, the gain adjustment should be set as follows (see Figure 7). Set the Hewlett-Packard 214A pulse generator for a pulse width of 50 us at 5,000 PPS with an output of 100 MV into the 100:1 voltage divider. Adjust the gain control on the Loop Amplifier for 5 volts as read on the Tektronix scope.

If the CW signal is being tracked across the band but does not meet the 2 MHz and 50 pulses requirement, the input power adjustment on the Phase Discriminator should be adjusted for optimum performance.



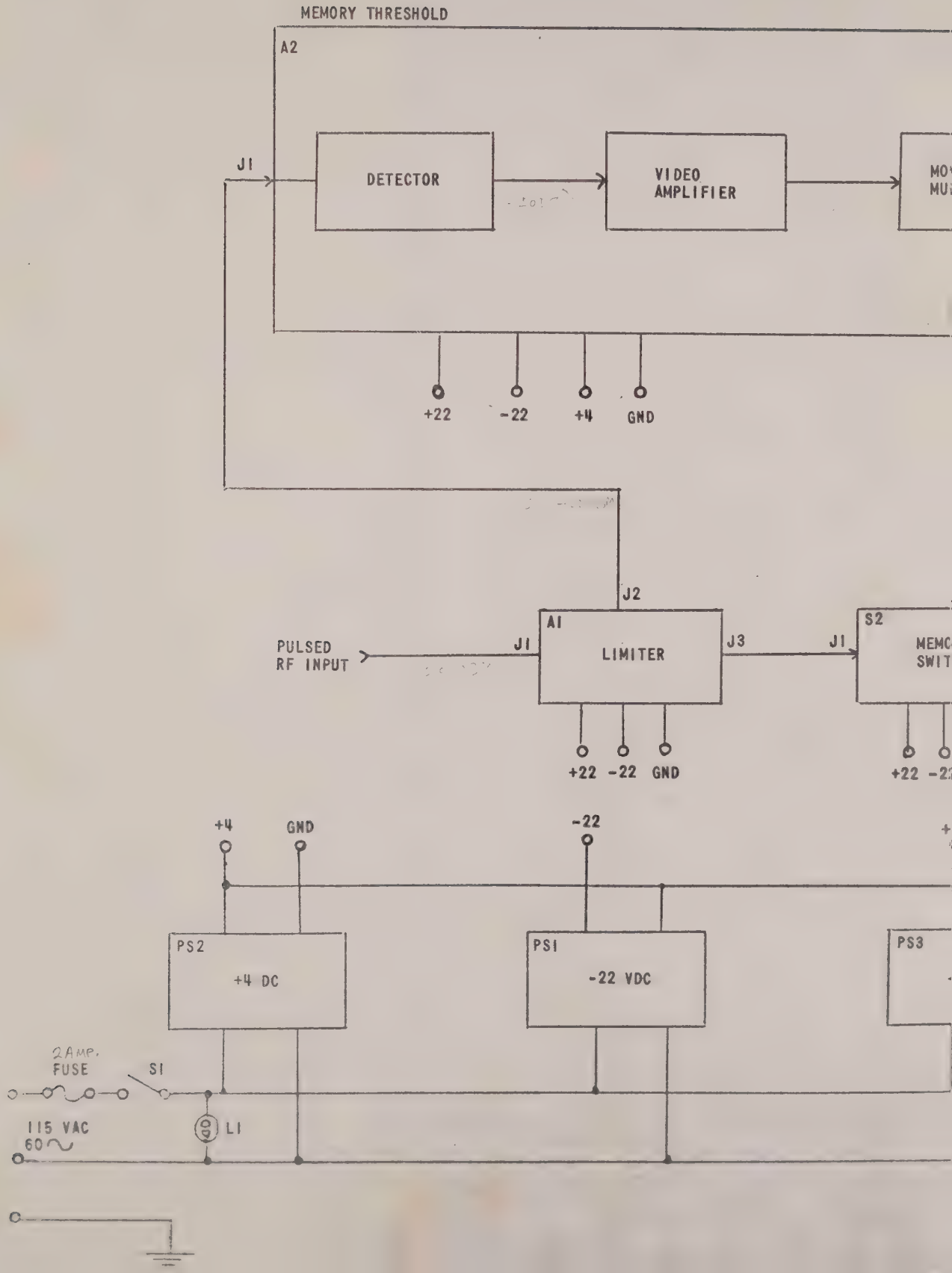
OVERALL ASSEMBLY

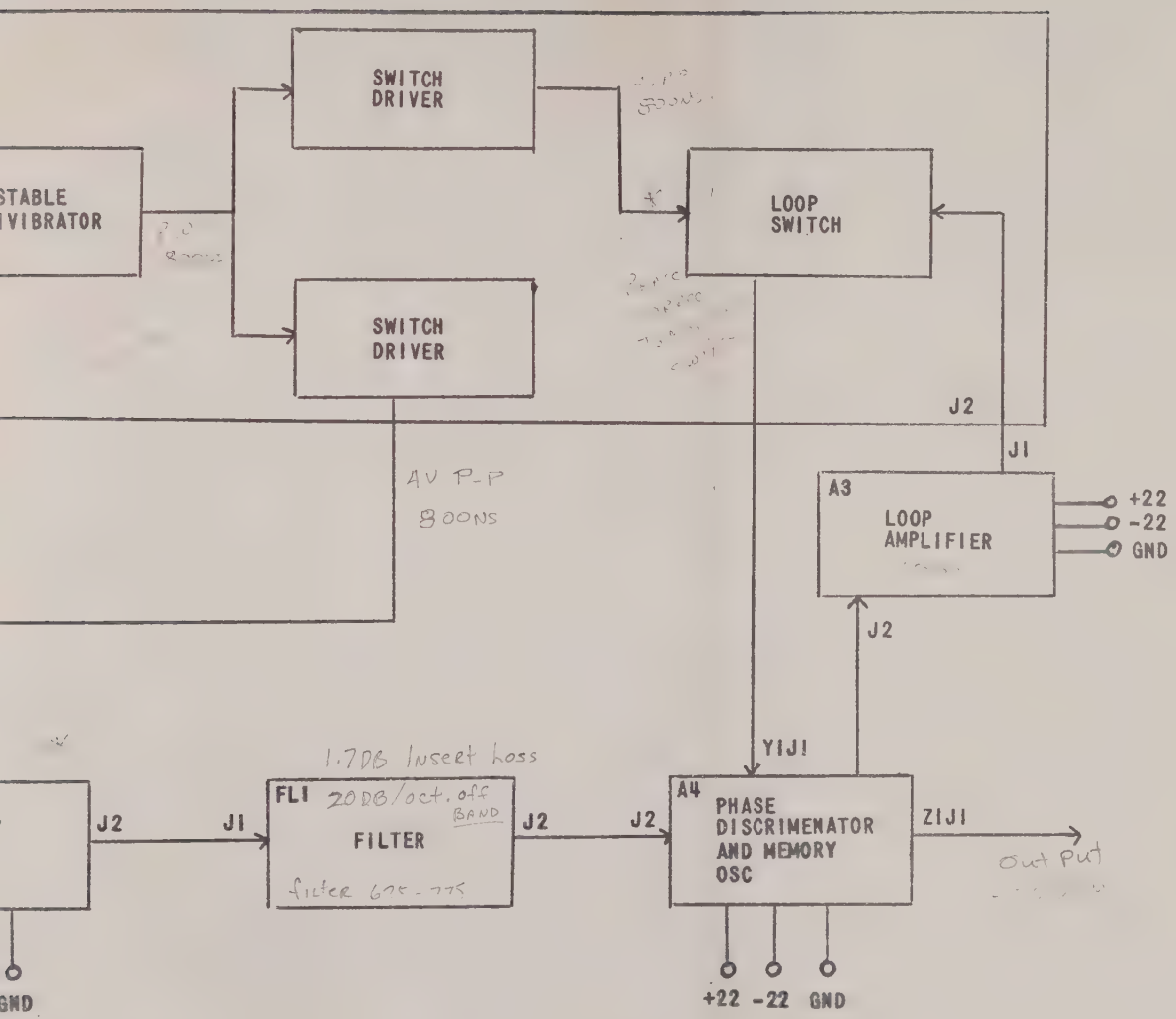
Figure 1



FREQUENCY ACCURACY & FREQUENCY ACQUISITION SETUP

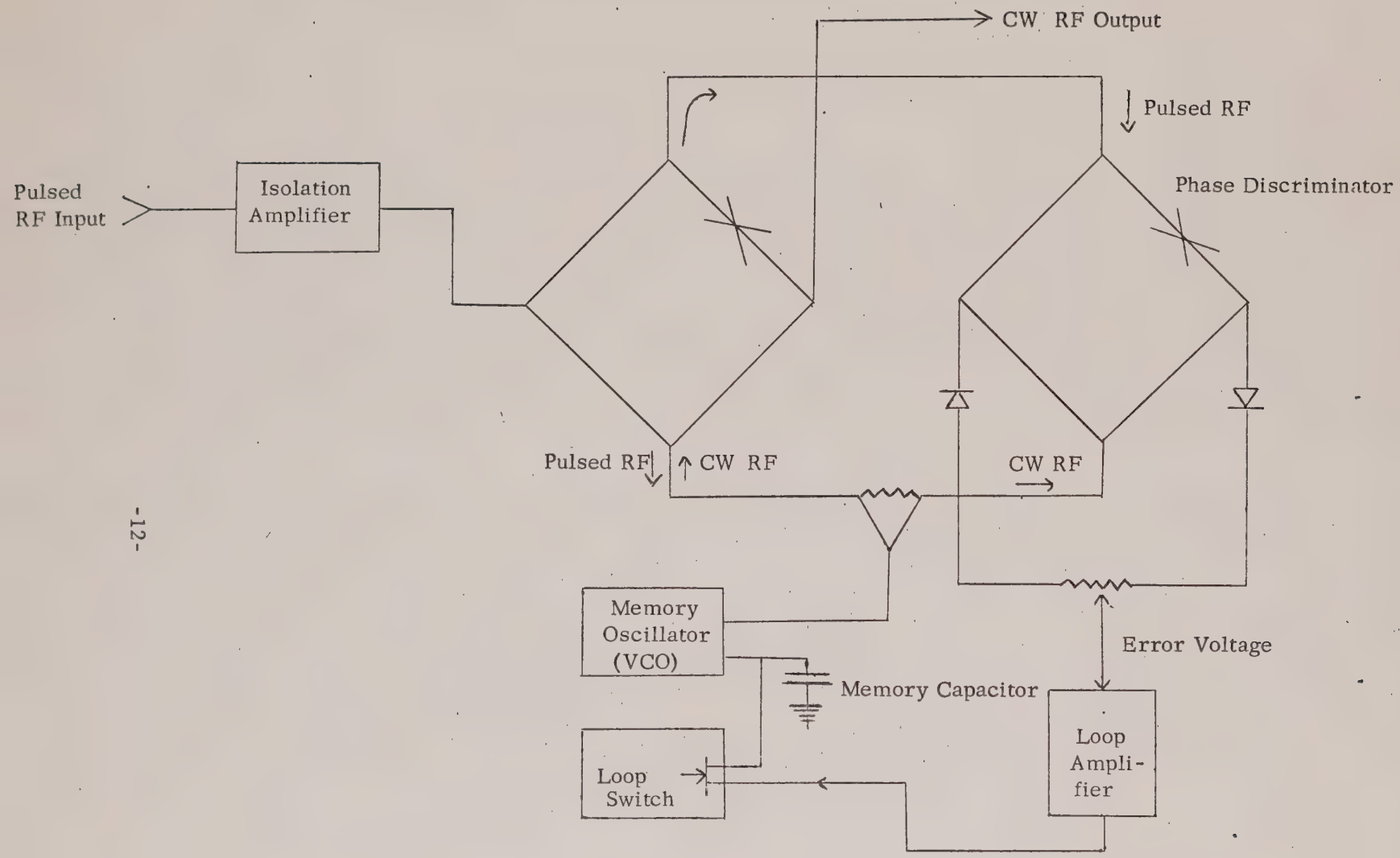
Figure 2


MEMORY THRESHOLD
A2
J1
DETECTOR
VIDEO AMPLIFIER
+22
-22
+4
GND
J2
A1
LIMITER
PULSED RF INPUT
J1
J3
J1
S2
+22
-22
GND
+4
GND
-22
PS2
+4 DC
PS1
-22 VDC
PS3
2 AMP. FUSE
S1
115 VAC 60~
L1



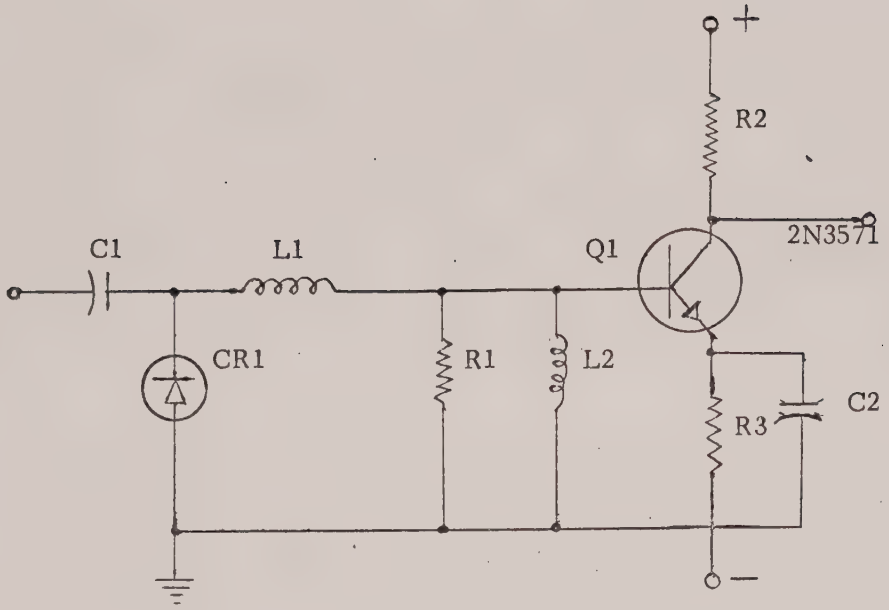
MODEL 4482 FREQUENCY MEMORY
BLOCK DIAGRAM

FIGURE 3



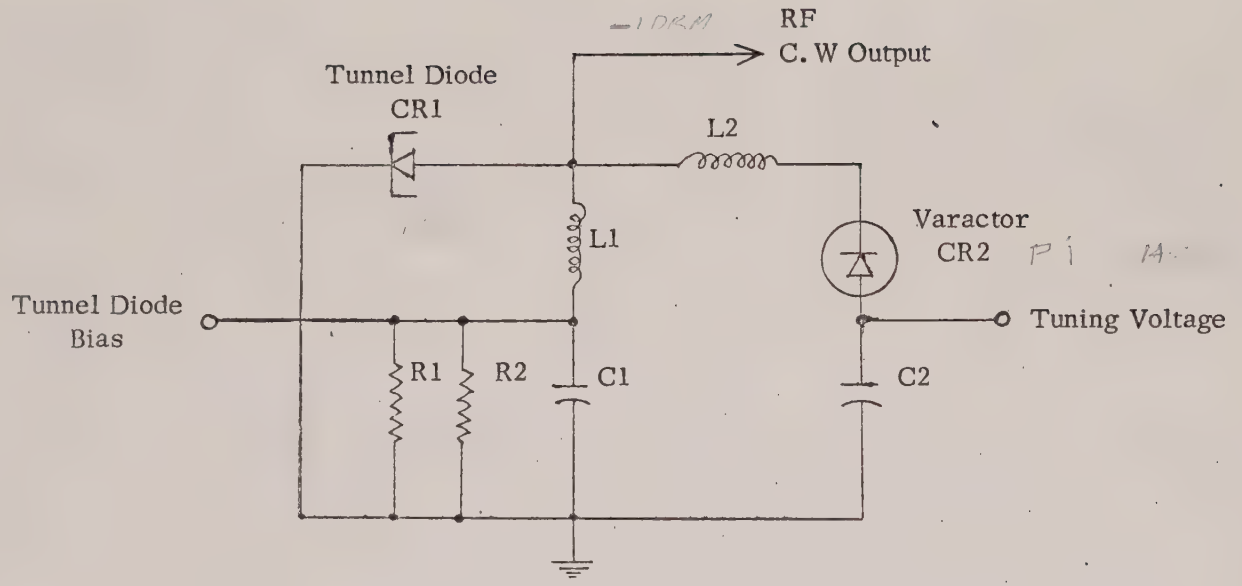
LOOP CIRCUITRY

Figure 4



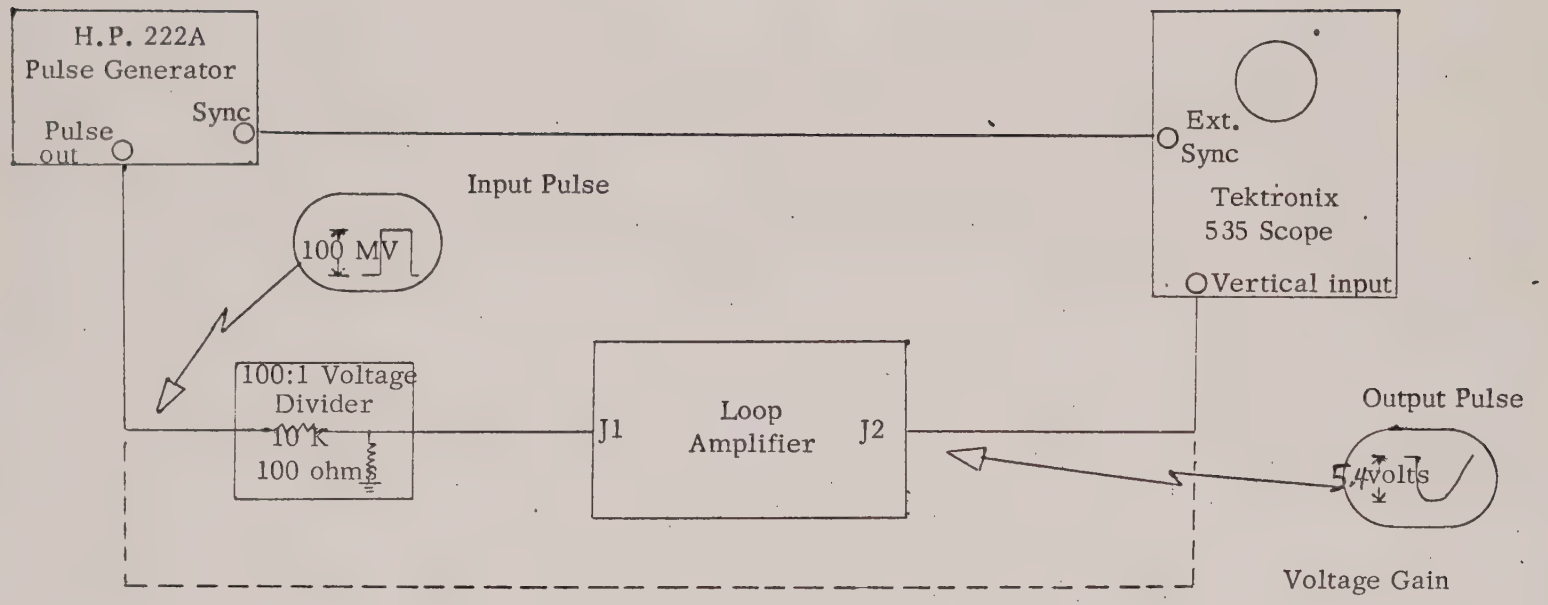
IF LIMITER STAGE

Figure 5



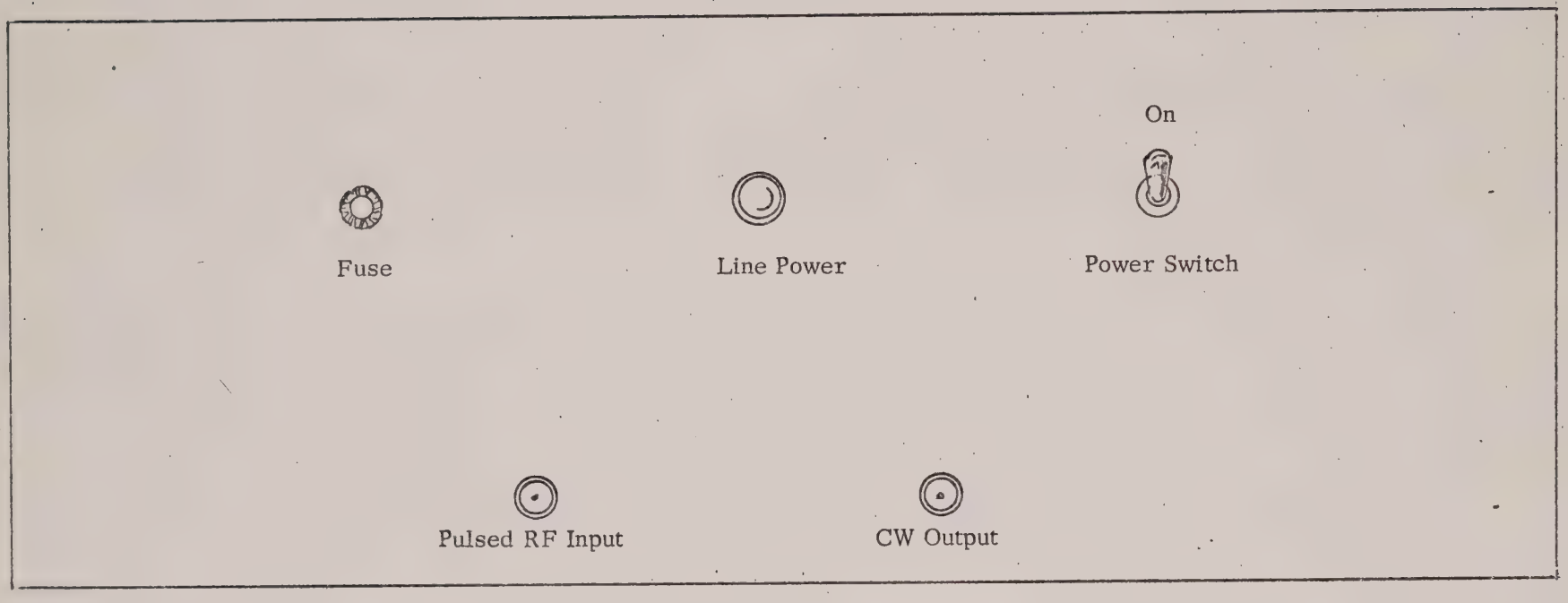
MEMORY OSCILLATOR

Figure 6



LOOP AMPLIFIER ADJUSTMENT

Figure 7



FRONT PANEL

Figure 8

SPECIFICATIONS

Frequency Range - 625-775 MHz

RF Input Pulse Width - 1.0 us or longer

RF Input Pulse Level - -25 dbm to 0 dbm

RF Output Level - -25 dbm $\pm$1 db

Number of Pulses Required for Initial Acquisition - 50 pulses maximum

Frequency Accuracy

(a) Immediately after RF pulse - $\pm$2 MHz

(b) Rate of frequency drift - 2 MHz/100 ms maximum (2 MHz/ 2 seconds typical)

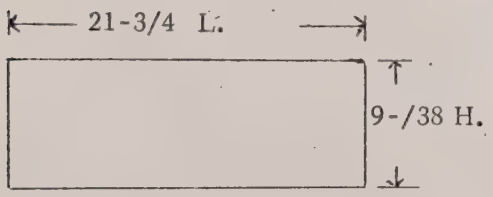
Pulse-to-Pulse Frequency Jump (Tuning Ability) - $\pm$5 MHz

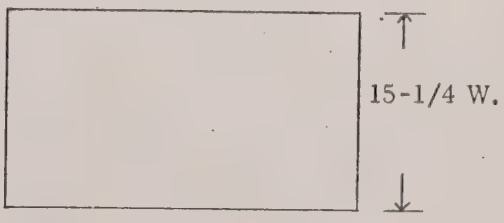
Spurious Outputs Within Frequency Range - Minimum of 20 db below desired signal

General

Power - 105-132 AC volts at 45-440 cps

Dimensions:





Equipment Required for Test and Adjustments

H.P. 612 RF generator or equivalent

H.P. 214A pulse generator

H.P. 851/8551 spectrum analyzer

DC voltmeter

Power Supply Voltage Adjustments

On each of the power supplies there is a control to adjust the DC output of the supplies. The control is on the front of the supply. The front panel has to be removed to adjust the supply voltages (by removing the four screws on the front panel).

Terminal Board - TBI

Wire	Voltage	Power Supply
Red	$\neq$ 22 volts	PS 1
Orange	$\neq$ 4 volts	PS 3
Purple	-22	PS 2
Black	Ground	

Color Code List

Red	$\neq$ 22 V	Black	Ground
Purple	-22 V	Gray	AC 110V
Orange	$\neq$ 4 V	Gray/White	AC neutral